REMARKS

Favorable reconsideration of this application is requested. Claims 1 and 2 remain pending. Editorial revisions have been made in claims 1 and 2. In addition, the location of the dummy bumps has been clarified, as supported for example by Figs. 3-5. The limitation concerning the height of the dummy bumps is supported, for example by the discussion in the specification of how the dummy bumps differ from the bonding bumps only in terms of area. Certain of the drawings have been labeled as prior art as requested.

The title of the application was considered objectionable. A new title has been provided. Applicant invites the Examiner's suggestion for a title if the new title is not considered adequate.

The drawings were found objectionable for not including the legend prior art where appropriate. Appropriate revisions have been made in the drawings.

Claims 1 and 2 were rejected as anticipated by JP 4-94732. Applicant traverses this rejection. This reference utilizes dummy bumps at the corners of the chip that will come into contact with the substrate before the remainder of the bonding bumps do. As a result, undesirable pressure is applied to the substrate at these locations. This fails to disclose or suggest the dummy bumps having the same height as the bonding bumps as required by claim 1. The rejection should be withdrawn.

Claims 1 and 2 were rejected as anticipated by JP 8-46313. Applicant traverses this rejection. This reference discloses dummy bumps that abut the edges of the chip. As a result, undesirable particles can be produced when the chip is separated from a wafer by dicing. This fails to disclose or suggest the bumps that are spaced from the edge as required by claim 1. The rejection should be withdrawn.

Claims 1 and 2 were rejected as anticipated by JP 2003-282812. Applicant traverses this rejection. The rejection is made under 35 USC 102(e). 35 USC 102(e) applies only to US patents or published applications. Therefore, the rejection is incorrect. The reference has a publication date for purposes of 35 USC 102(a) of October 3, 2003, which is subsequent to the October 31, 2002 priority date of the present application. A verified translation of the priority application will be submitted shortly to perfect the claim for priority.

Claims 1 and 2 were rejected as anticipated by JP 9-115910. Applicant traverses this rejection. This reference discloses bumps located at a central portion of the semiconductor chip. Thus, the reference does not disclose and is not relevant to issues involving devices in which the bumps are provided at a peripheral edge as required by claim 1.

Claims 1 and 2 were rejected as anticipated by US 6,287,895. Applicant traverses this rejection. Fig. 1A of the reference discloses an embodiment in which the dummy bump is higher than the active bumps. This fails to disclose or suggest claim 1 for the reasons discussed above relative to JP 4-94732. The remaining figures in the reference show protective dummy members that abut the edges of the device. This fails to disclose or suggest claim 1 for the reasons discussed above relative to JP 8-46313.

Favorable reconsideration in the form of a Notice of Allowance is requested.

Respectfully Submitted,

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Dated: October 29, 2004

By _____
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IN THE DRAWINGS

Replacement sheets for Figs. 1, 2, 7(a), 7(b) and 8 are provided herewith in formal form. The figures have been revised to include the legend "prior art" as requested.